CSCI E-93, Spring 2026: Computer Architecture

Prof. James L. Frankel
Harvard University

First Class Meeting on 1/27/2026

First Class Meeting Agenda

- Class website & Canvas, Zoom links
- Staff introductions
- Polls
- Student introductions
- Class website & class information
- Student actions: Order books, Say Hello!, Student Locations, HarvardKey, Cisco AnyConnect VPN, cscie93.dce.harvard.edu instance, order hardware
- Course problem set overview
- Problem Sets 0 & 1
- Digital electronics & Boolean logic

Class Website, Canvas, Zoom Links

- Our **class website** is located at URL:
  https://cscie93.dce.harvard.edu/spring2026/

- Please participate in the live stream and ask questions verbally using **Zoom** available in **Canvas** (**https://canvas.harvard.edu/courses/166213**) under the **Zoom** menu

- In addition, questions may be asked textually using **Zoom's Chat facility**

Zoom

- You are encouraged to turn on your video feed
  - This allows the course staff to better determine if students seem puzzled and/or if they have questions

- Class and section meetings are recorded
  - Students who are unable to attend a meeting for any reason are able to view recordings later
  - It's still better to participate in the live session so that questions can be asked and answered
  - Many students find that reviewing material later to fully appreciate the details presented during class – even if they participated in the live class – is very helpful

Staff Introductions

- Professor
  - James "Jamie" Frankel

- Teaching Assistants
  - Mark Ford
  - Stephen Benjamin

Quick Polls

- Goals and Interest for Class Enrollment (Multiple Choice)
- Class Participation
- Section Participation
- Class Expectations (Multiple Choice)

- You can choose to answer the polls anonymously

Student Introductions

- Please tell us a little about yourself
  - Where you're located
  - What you do when you're not at Harvard
  - Your technical background
  - Your out-of-work/school hobbies

Tour of Class Website

- At the top there are alerts in red

- Quick Links

- Links for streaming and videos

- Info about midterm exam, prerequisites, overview, bibliography, instructors and section, Ed Discussion wiki/forum, Say Hello!, your location, git & GitHub, grading, accessibility, plagiarizing, publishing/distributing course materials, outline/approximate schedule, hardware-related information, agenda for the upcoming class, slides used in class, questionnaire & problem sets, assorted links, link to the section home page

Meeting Times

- Section meets on Tuesdays in Room L01, 53 Church Street, Harvard Square, Cambridge, Massachusetts from 6:45 PM to 7:45 PM Eastern Time (ET) and in Zoom using the **Section: HELIX Classroom room**
  - This is immediately before class meets

- Class meets on Tuesdays in Room L01, 53 Church Street, Harvard Square, Cambridge, Massachusetts from 8:00 PM to 10:15 PM Eastern Time (ET) and in Zoom using the **Class: HELIX Classroom room**
  - Elongated class meeting time

- I will attempt to include a break during the class meetings *(but no guarantee because of scope of material to be presented)*

Section

- Required part of class

- Very important
  - Discusses concepts & issues that are not covered in class
  - Often gives a sketch of algorithms and approaches to be used in solving the problem sets
  - Adds enrichment on topics discussed in class/lecture

  - Great forum for a more interactive dialog

  - Is live streamed and also recorded

DCE Course Listing

- Course Listing is available at
  https://courses.dce.harvard.edu/?details&srcdb=202602&crn=27072

- Simple Syllabus is available at https://harvard.simplesyllabus.com/en-US/syllabus/Spring%20Term%202026%20-%20Full%20Term/CSCI/E-93/1

Class Website Review

- Questions?
  - Questions are always welcomed
    - Any questions now?
  - If there is limited time to answer questions, I'll let you know

- Review of Class Website
  - Midterm exam
  - Prerequisites
  - Overview
  - Required and optional books
  - The daily agenda (these slides) and all slides used in class
  - …

- Order books, if you have not already done so
  - Contemporary Logic Design, 2/e; Katz & Borriello
  - Computer Organization and Design: The Hardware/Software Interface, MIPS Edition, 6/e; Patterson & Hennessy
  - The Designer's Guide to VHDL, 3/e; Ashenden
- Somewhat limited online access is available to all of our books through our Library Reserves link in Canvas
  - Katz & Borriello and Patterson & Hennessy (and perhaps others) are available for just three hours at a time

Required Readings

- Refer to the Approximate Schedule section of the course website for required readings to be completed before each class meeting

Say Hello!, Student Locations, Harvard Key, Using cscie93.dce.harvard.edu

- Submit a video in Canvas under **Discussions** as a reply to my "Say Hello!" topic

- Please post your primary location using **Student Locations** facility in Canvas

- Ensure that your **Harvard Key** is established

- Ensure that you are able to VPN into Harvard using vpn.harvard.edu and Cisco AnyConnect

- Ensure that you have an account on our cscie93.dce.harvard.edu AWS instance
  - **Once your VPN connection is established**, login to cscie93.dce.harvard.edu using SSH/SFTP (SecureCRT & SecureFX) with your HarvardKey NetID as your login name and your HarvardKey password as your password
  - If you are unable to login to cscie93.dce.harvard.edu, you may need to synchronize your HarvardKey password by using a browser to visit https://key.harvard.edu/manage-account and then clicking on "Synchronize Password >" and following the instructions on the next screen

g.harvard.edu e-mail Address

- If you're interested, you can get a g.harvard.edu account that will give you a *logname*@g.harvard.edu e-mail address and access to Google Apps for Harvard
    - Get started at http://g.harvard.edu/
    - Note: Please be aware that when you claim your g.harvard account that g.harvard will become your primary Harvard e-mail address. All official communication from Harvard will be sent to your new g.harvard address and your g.harvard account will become your HarvardKey login name.

Class Discussion Group: Ed Discussion

- Ask all non-personal questions in Ed so the whole class can benefit from the answers
  - Ed can be found in Canvas by following the Ed Discussion link (https://canvas.harvard.edu/courses/166213/external_tools/121327?display=borderless)
  - Students are welcome to answer questions there, too
  - Personal questions should be sent to the course staff via e-mail
    - If appropriate, include all three course staff members in e-mail to allow the fastest reply
  - All registered students should already be in our Ed group

- To **receive immediate notifications about new threads:** in our Ed group, in the upper right, click on the **Account** icon, then…
  - Select **Settings**
  - Click on **Notifications**
  - Change the frequency to receive e-mails about new threads to **Instant**
  - Also, ensure that all other **Notification Emails** are active

Intel/Altera/Terasic DE2-115 Hardware

- Show class the hardware
  - If the Intel/Altera DE2-115 FPGA is available, students should order the hardware immediately
    - **Intel/Altera DE2-115 FPGA kit**
    - Note: Terasic has announced the discontinuation of the DE2-115 board. Because of the number of slide switches, pushbuttons, LEDs, seven-segment LEDs, etc., this board is crucial for this course. Therefore, if available from another vendor, order the hardware immediately.
    - Listing on **Terasic** (http://www.terasic.com.tw/en/ & https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=165&No=502)
    - Academic pricing is available (US$779 usual; US$423 academic) – Great deal!
    - Valid student ID card or a screen shot that shows that you're registered in the course is sufficient to get the academic pricing
  - Students who are unable to order the hardware, may borrow hardware for the duration of the semester, but **must return the hardware promptly** after the semester ends
  - An inventory will determine how many DE2-115 kits are available
  - In addition to Terasic FPGA board, order **USB to serial adapter** & **serial cable**
  - Optional **static dissipative devices**: mat, strap, ground point

Midterm Exam

- Our **midterm exam** will be available starting at **8:00 PM ET on March 10, 2026**
  - The exam must be started within 24 hours of the date & time above
  - The exam is three hours in length
  - The exam will be administered under Proctorio
- There will be **no class meeting on March 10th**, but **section will still be held on March 10th**
  - No topics relevant to the midterm exam will be discussed in that section meeting

Problem Set Overview

- Problem Set 0: the course questionnaire, fix-this-program & word-count
- Problem Set 1: textbook problems from Katz & Borriello
- Problem Set 2: block diagram & instruction set
- Problem Set 3: VHDL counter, textbook problems from Katz & Borriello, final program in the C Programming Language
- Problem Set 4: assembler, final program in your assembly language
- Preliminary Final Project Problem Set (ALU)
- Problem Set 5: emulator
- Problem Set 6: sequencer action description, VHDL memory system interaction
- Final Project: VHDL processor design

Five Free Late Days

- Please don't use any of your five free late days early in the class
- Because the later problem sets are built upon earlier problem sets, the free late days are more valuable later in the semester
- Also, the larger problem sets are worth more points and take much more time to complete

Problem Set 0

- Complete Problem Set 0
  - Establish a GitHub account
  - Install git as described on the section website (https://cscie93.dce.harvard.edu/spring2026/section/index.html)
  - Modify the course questionnaire with your personal answers
  - Fix warnings and errors in fix-this-program on the cscie93 instance
  - Write the word count program
  - Create a branch named "problem-set-0", create a merge request, add the appropriate comment

- Due this coming Sunday night, February 1st, 2026 at midnight ET

Problem Set 1

- Present **Problem Set 1**
  - Due at midnight ET on Sunday night, February 8th, 2026

Lying to Students

- I will lie to you this semester

Lying to Students

- I will lie to you this semester
    - There are too many details to give the whole truth
    - That is the only way we can make reasonable progress through the material

- By the end of the semester, all lies will be fully corrected

Non-academic Class Activities

- Encourage a student community

- If interested, students are welcome to gather with us after each class for dinner in Cambridge
  - Opportunity for students to socialize in an informal setting outside of class
  - Discussion/conversation/sharing after class
  - Not relevant to class

- Other non-class activities
  - Class ski trip in January
  - Sailing trip in the summer

Class Break

- Let's take a 10 minute break

- You're welcome informally interact during the break

Today's New Material

- Cover **Binary Logic Levels** slides through slide **#2** (except for the last bullet point)

Second Class Meeting on 2/3/2026

Second Class Meeting Agenda

- Questions and Comments
- Administrivia
  - Start work on problem sets early
  - Section
  - Status of Terasic orders
  - Intel/Altera/Terasic DE2-115 Hardware
  - Intel/Altera Quartus FPGA Design Software
  - Student Locations
  - Say Hello! in Canvas
  - Class Discussion Group: Ed Discussion
- Current Problem Set Status
- Boolean Logic Levels (continued)
- Boolean Logic
- Boolean Logic Continued
- Advanced Boolean Logic
- Laws and Theorems of Boolean Logic
- Gray Codes & Karnaugh Maps
- Computer Logic

Questions and Comments

- Section
- Last week's class
- Problem Sets 0 & 1
- Access to the class cscie93.dce.harvard.edu instance
- Ed Discussion threads
- Readings
- Anything else

Start Work on Problem Sets Early

- In order to ensure that your questions are answered in a timely manner, start work on problem sets early

- The course staff are often quite prompt in answering Ed questions, but there is no guarantee of immediate responses

Section

- **Required part of class**
- Section meets immediately before class on Tuesdays from 6:45 PM to 7:45 PM Eastern Time (ET) and in Zoom using the **Section: HELIX Classroom room**

- Very important
  - Discusses concepts & issues that are not covered in class
  - Often gives a sketch of algorithms and approaches to be used in solving the problem sets
  - Adds enrichment on topics discussed in class/lecture

  - Great forum for a more interactive dialog

  - Is live streamed and also recorded

Status of Terasic Orders

- Everyone who wants to order hardware should do so now
- Problem Set 3 (due on March 8, 2026) is the first problem set that requires the hardware

- If you are not able to or do not want to purchase hardware, I will be able to **distribute hardware** during our fourth class meeting on **Tuesday, February 17, 2026** to students who are local to Cambridge/Boston
  - I will be able to send hardware to students via FedEx
- If you want to borrow hardware for your use during the semester, you must let me know as soon as possible

Intel/Altera/Terasic DE2-115 Hardware

- Show class the hardware
  - All students should order the hardware **immediately**
    - **Intel/Altera DE2-70 or DE2-115 FPGA kit**
    - Note: Terasic has discontinued both the DE2-70 and DE2-115 boards. Because of the number of slide switches, pushbuttons, LEDs, seven-segment LEDs, etc., these boards are crucial for this course. Therefore, order the hardware immediately.
    - See **Terasic** (http://www.terasic.com.tw/en/ & https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=165&No=502)
    - Academic pricing was available (US$779 usual; US$423 academic) – Great deal!
  - Students who are unable to order the hardware, may borrow hardware for the duration of the semester, but **must return the hardware promptly** after the semester ends
  - In addition to Terasic FPGA board, order **USB to serial adapter** & **serial cable**
  - Optional **static dissipative devices**: mat, strap, ground point

Intel/Altera Quartus FPGA Design Software

- The most recent version of Quartus that supports the Altera DE2-115 boards (with a Cyclone IV FPGA) is Quartus Prime Lite Edition, Release 20.1.1
  - **All of us will be using Quartus Prime Lite Edition, Release 20.1.1**
- For release 20.1.1, only the Lite Edition can be utilized for free – it doesn't require a License Key
- Only 64-bit x86 processors running Windows are supported
  - You **are** able to use a VM under MacOS
  - You **are not** able to run Quartus under a VM on any Apple ARM (Apple Silicon) processors
  - Windows 10 is available for free from Microsoft
- **You need to have a 64-bit x86 processor or VM running Windows**

Student Locations

- Please post your primary location using **Student Locations** facility in Canvas

Say Hello! in Canvas

- Submit a video in Canvas under **Discussions** as a reply to my "Say Hello!" topic

Class Discussion Group: Ed Discussion

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  - Click on **Notifications**
  - Change the frequency to receive e-mails about new threads to **Instant**
  - Also, ensure that all other **Notification Emails** are active

Current Problem Set Status

- **Problem Set 0 was due** this past Sunday night

- Go over **Problem Set 1**
  - All book problems from Katz and Borriello
  - Due at midnight ET on this coming Sunday, February 8th, 2026

- I will present **Problem Set 2** in class next week

Today's New Material

- Finish covering **Binary Logic Levels** slides
  - Cover **Binary Logic Levels** slides beginning with the last bullet point in slide **#2**

- Cover new slides
  - Cover **Boolean Logic** slides
  - Cover **Boolean Logic Continued** slides
  - Cover **Advanced Boolean Logic** slides
  - Cover **Laws and Theorems of Boolean Logic** slides
  - Cover **Gray Codes & Karnaugh Maps** slides
  - Cover **Computer Logic** slides